CLAIMS

What is claimed is.

1. A ball-limiting metallurgy (BLM) stack comprising:

a metal adhesion first layer disposed above and on a metallization;

a metal second layer disposed above and on the metal adhesion first layer;

a metal third layer disposed above and on the metal second layer;

an electrically conductive bump disposed above and on the metal third layer; and

wherein at least one of the metal second layer and the metal third layer comprises copper.

2. The BLM stack according to claim 1, wherein the metal adhesion first layer is selected from Ti, TiW, W, and Cr.

3. The BLM stack according to claim 1, wherein the metal second layer comprises copper and the metal third layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy.

4. The BLM stack according to claim 1, wherein the metal second layer comprises copper and the metal third layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-solution or stoichiometric ratio.

5. The BLM stack according to claim 1, wherein the metal second layer comprises copper and the metal third layer is selected from a nitrided refractory metal, a nitrided metal-doped refractory metal, or a nitrided refractory metal alloy selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-solution or stoichiometric ratio.

6. The BLM stack according to claim 1, wherein the metal third layer comprises copper, and wherein the metal second layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy.

7. The BLM stack according to claim 1, wherein the metal third layer comprises copper and the metal second layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-solution or stoichiometric ratio.

8. The BLM stack according to claim 1, wherein the metal third layer comprises copper and the metal second layer is selected from a nitrided refractory metal, a nitrided metal-doped refractory metal, or a nitrided refractory metal alloy selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-solution or stoichiometric ratio.

9. The BLM stack according to claim 1, wherein the metal second layer comprises a copper layer and wherein the metal third layer comprises a copper stud

10. The BLM stack according to claim 1, further comprising:

an intermetallic layer disposed between the metallization and the electrically conductive bump.

11. The BLM stack according to claim 1, wherein the electrically conductive bump comprises a tin-lead solder composition selected from Sn37Pb, Sn97Pb, and Sn_xPb_y, wherein x+y total 1 and wherein x is in a range from about 0.3 to about 0.99.

12. A process comprising:

forming a metallization over a substrate;

forming a metal adhesion first layer above and on the metallization;

forming a metal second layer above and on the metal adhesion first layer;

forming a metal third layer above and on the metal second layer;

forming a solder bump above and on the metal third layer, and

wherein at least one of the metal second layer and the metal third layer comprises sputtered copper.

13. The process according to claim 12, forming a metal adhesion first layer further comprising:

sputtering a composition over the metallization under conditions to impart a compressive stress in the metal adhesion first layer, wherein the composition is selected from Ti, TiW, W, and Cr.

14. The process according to claim 12, forming the metal second layer and forming the metal third layer further comprising:

sputtering a copper metal second layer over the metal adhesion first layer under conditions to impart a compressive stress therein; and

sputtering the metal third layer under conditions to impart a compressive stress therein, wherein the metal third layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy.

15. The process according to claim 12, forming the metal second layer and forming the metal third layer further comprising:

sputtering the metal second layer over the metal adhesion first layer and under conditions to impart a compressive stress therein, wherein the metal third layer is selected from a refractory metal, a metal-doped refractory metal, or a refractory metal alloy; and

sputtering a copper metal third layer over the metal second layer under conditions to impart a compressive stress therein.

16. The process according to claim 12, forming the metal second layer and forming the metal third layer further comprising:

sputtering a copper metal second layer over the metal adhesion first layer under conditions to impart a compressive stress therein; and

plating a copper stud through a mask that is disposed over the metal second layer.

17. The process according to claim 12, further comprising:

forming an electrically conductive bump above and on the metal third layer.

18. A process comprising:

forming a copper pad over a metal-six (M6) metallization;

sputtering a Ti metal adhesion first layer above and on the metallization;

sputtering a metal second layer above and on the Ti metal adhesion first layer;

forming a metal third layer above and on the metal second layer;

forming a solder bump above and on the metal third layer, and

wherein at least one of the metal second layer and the metal third layer comprises copper.

19. The process according to claim 18, wherein sputtering a Ti metal adhesion first layer above and on the metallization comprises:

sputtering a Ti composition over the metallization, wherein the Ti composition has a thickness in a range from about 500 Å to about 4,000 Å.

20. The process according to claim 18, wherein sputtering a metal second layer and forming a metal third layer comprise:

sputtering a NiV composition over the Ti metal adhesion first layer, wherein the NiV composition has a thickness in a range from about 1,000 Å to about 5,000 Å; and

sputtering a Cu composition over the metal second layer, wherein the metal third layer has a thickness in a range from about 1,000 Å to about 5,000 Å.

21. The process according to claim 18, wherein forming a metal third layer comprises:

sputtering a NiV composition over the metal second layer, wherein the NiV composition has a thickness in a range from about 1,000 Å to about 5,000 Å, and wherein the metal second layer has a thickness in a range from about 1,000 Å to about 5,000 Å.

22. The process according to claim 18, wherein forming a metal third layer comprises:

electroplating a copper stud over the metal second layer, wherein the copper stud has a thickness in a range from about 5 micrometers to about 15 micrometers, and wherein the metal second layer has a thickness in a range from about 1,000 Å to about 5,000 Å.

23. A system comprising:

a substrate comprising an electrical device;

a metallization pad disposed over the substrate;

a ball-limiting metallurgy disposed over the metallization pad, the ball-limiting metallurgy comprising:

a metal adhesion first layer disposed above and on the metallization pad;

a metal second layer disposed above and on the metal adhesion first layer;

a metal third layer disposed above and on the metal second layer;

an electrically conductive bump disposed above and on the metal third layer;

wherein at least one of the metal second layer and the metal third layer comprises copper; and

a flip-chip disposed over the ball-limiting metallurgy.

24. The system according to claim 23, wherein the flip-chip comprises a solder having a composition of about Sn37Pb, and wherein the electrically conductive bump comprises a solder having a composition of about Sn97Pb.

25. The system according to claim 23, wherein the electrical device comprises a chip-scale package.

26. The system according to claim 23, wherein the flip-chip comprises a chip-scale package.

27. The system according to claim 23, wherein the electrical device comprises a chip-scale package and wherein the flip-chip comprises a chip-scale package.

28. The system according to claim 23, further comprising:

an intermetallic zone that substantially isolates the metal third layer from the electrically conductive bump.

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